What Is Claimed Is:

1. A method for processing operands in a processing unit having at least two execution units, which are able to be operated at a predefinable clock cycle, the execution units being triggered by control signals for the processing of the operands, and a switch may be made between a first operating mode and a second operating mode, wherein in the first operating mode both execution units are supplied with the same operands and in the second operating mode both execution units are supplied with different operands, and both execution units are triggered by the same control signals for the processing of the operands in the first operating mode, and both execution units are controlled by different control signals for the processing of the operands in the second operating mode.

2. The method as recited in Claim 1, wherein the operands are supplied to the execution units as a function of the clock cycle for operand processing of the execution units in the form of a full cycle, and in the second operating mode the operands are supplied at a second clock cycle for the processing of the operands, the second cycle being faster than the full cycle.

3. The method as recited in Claim 2, wherein in the first operating mode the operands are supplied at the clock cycle of the execution units, as full cycle.

4. The method as recited in Claim 2, wherein, compared to the full cycle, the faster second clock cycle is designed as half cycle and is twice as fast.

5. The method as recited in Claim 1, wherein the execution units process the operands in synchrony in both operating modes.

6. The method as recited in Claim 1, wherein the operands are processed in synchrony in the first operating mode and in asynchrony in the second operating mode.

7. The method as recited in Claim 1,
wherein the operands, or data derived from the operands, are compared for agreement and an error is detected in case of a deviation.

8. The method as recited in Claim 1,
wherein states or results (result A, result B) produced in the processing of the operands are compared for agreement and an error is detected in a deviation, the comparison being implementable as a function of the individual operating mode.

9. The method as recited in Claim 8,
wherein the states or results are released by a release signal as a function of the operating mode and the comparison.

10. The method as recited in Claim 9,
wherein the states or results are released by the release signal simultaneously or successively as a function of the operating mode.

11. A device for operand processing in a processing unit having at least two execution units, which are able to be operated at a predefinable clock cycle, a control unit being included, which triggers the execution units by control signals for the processing of the operands and which switches between a first operating mode and a second operating mode,
wherein the control unit is connected to the execution units and additional feed units and the control unit cooperates with the feed units in such a way that both execution units are supplied with the same operands in the first operating mode and both execution units are supplied with different operands in the second operating mode, the control unit being designed such that both execution units are triggered by identical control signals for the processing of the operands in the first operating mode and both execution units are triggered by different control signals for the processing of the operands in the second operating mode.

12. The device as recited in Claim 11,
wherein the control unit and the feed units are designed such that in the first operating mode the operands are supplied to the execution units as a function of the clock cycle of the execution units, as full cycle, and in the second operating mode the operands are supplied for processing at a second clock cycle, which is faster than the full cycle.

13. The device as recited in Claim 11,
wherein the at least two execution units are embodied as arithmetic logic units (ALU A, ALU B).

14. The device as recited in Claim 11,
wherein the feed units and the execution units are designed such that in the first operating mode they operate or are operated in synchrony using an identical clock cycle.

15. The device as recited in Claim 11,
wherein the feed units as register system are designed such that at least one operand register is provided and at least one buffer register is provided between operand register and each execution unit.

16. The device as recited in Claim 11,
wherein the feed units and the execution units are designed such that they operate or are operated at different clock cycles in the second operating mode.

17. The device as recited in Claim 11,
wherein the feed units are designed such that in the second operating mode they operate or are operated at a clock cycle that is twice as fast as that of the execution units.

18. The device as recited in Claim 11,
wherein a decoder is provided by which a switchover condition is detectable, and the decoder operates, or is operated, at the same clock cycle as the feed unit.

19. The device as recited in Claim 11,
wherein comparison means are provided, which are designed such that the operands or data derived from the operands are compared for agreement and an error is detected in case of a deviation.

20. The device as recited in Claim 11,
wherein comparison means are provided, which are designed such that states or results (result A, result B) produced in the processing of the operands are compared for agreement and an error is detected in case of a deviation.

21. The device as recited in Claim 11,
wherein first switching means are provided, which are designed or able to be operated such that they switch the operands from the feed means as a function of the first or second operating mode.

22. The device as recited in Claim 11,
wherein second switching means are provided, which are designed or able to be operated in such a way that they activate the execution units as a function of the first or second operating mode.

23. A processing unit having a device for operand processing having at least two execution units, which are able to be operated at a predefinable clock cycle, a control unit being included, which triggers the execution units by control signals for the processing of the operands and which switches between a first operating mode and a second operating mode,
wherein the control unit is connected to the execution units and additional feed units and the control unit cooperates with the feed units in such a way that both execution units are supplied with the same operands in the first operating mode and both execution units are supplied with different operands in the second operating mode, the control unit being designed such that in the first operating mode both execution units are triggered by the same control signals for the processing of the operands and in the second operating mode both execution units are triggered by different control signals for the processing of the operands.

24. The processing unit as recited in Claim 23, having a device as recited in one of the Claims 12 through